IDEC Chip Design Contest

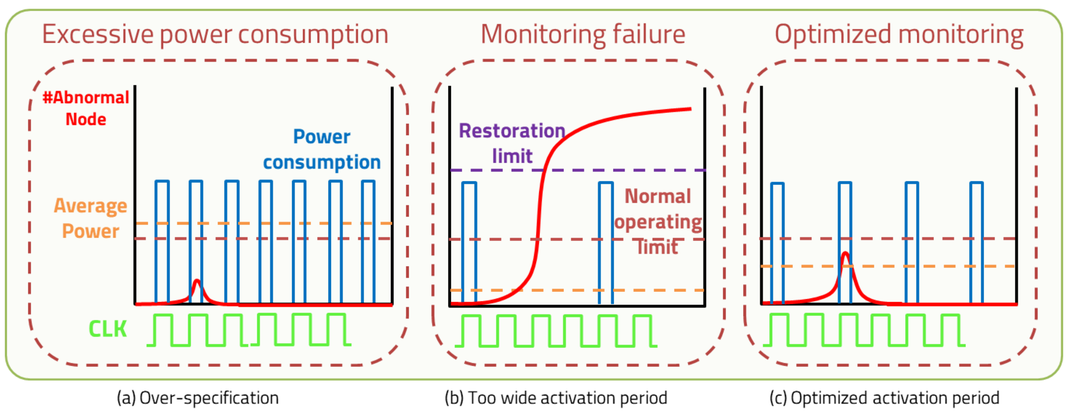
Low-Power Freeze-Safe IoT-Driven Processor based on RISC-V using Large-Scaled Heterogeneous Co-Simulation Method

Hyeon-gyun Moon and Daejin Park*
Sch. of Electronics Engineering, Kyungpook National University (KNU) boltanut@knu.ac.kr*

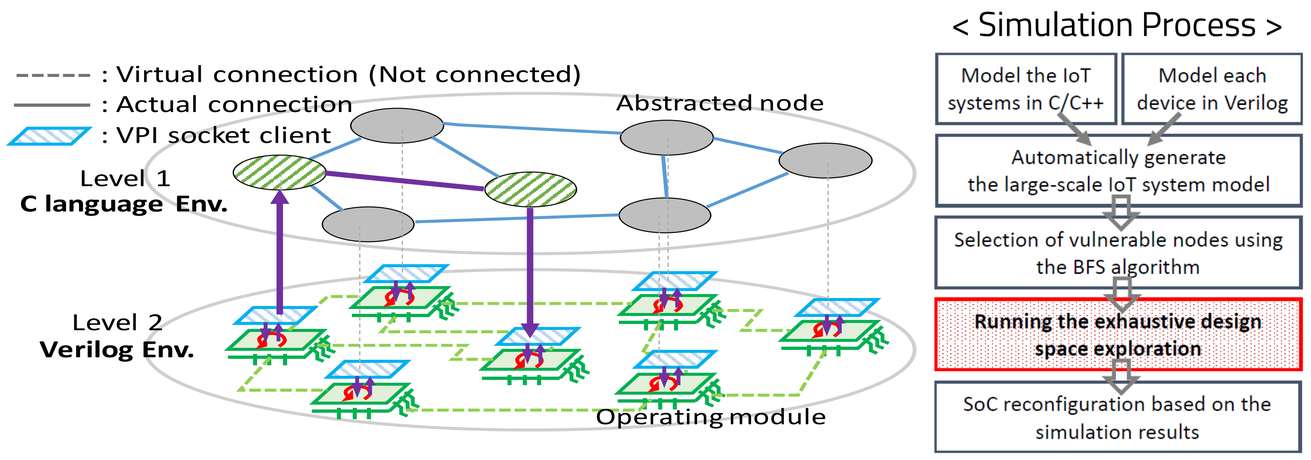
Abstract

IoT systems, which are connected with irregular links between heterogeneous things, are vulnerable to fast error propagation caused by unwanted abnormal statuses. We often add system monitoring circuits to protect against unresolved freezing due to this problem. However, practical approaches in the field result in the over-specification of designs to cover all unknown problems, so that a large amount of additional power is consumed. In this paper, we adopt two ways to solve this problem efficiently: the effective reconfiguration of power state parameters for the low-power operations of embedded hardware and software in a communication-centric system-on-chip (SoC), and a design-space-exploration framework under the large-scale construction of irregular links between the processors. Given the large-scale connection of SoCs for the experiment, the system can be safely operated with a very wide monitoring active cycle, and power consumption can also be reduced.

Proposed Fault-Safe IoT Platform



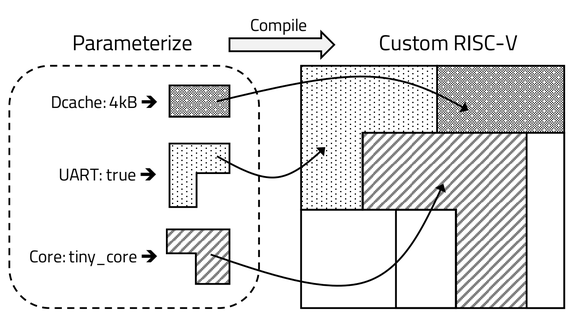
IoT system is difficult to monitor optimally due to complicated connectivity and numerous devices As a result, the power consumption may increase due to excessive monitoring as in (a), or the monitoring may fail as in (b), We need to find an optimal monitoring period that can operate with minimal power within the normal operating range of the system as shown in (c)



Through the heterogeneous co-simulation, Complex IoT systems can easily be represented in C/C++, graph structure, and HDL modules are automatically generated based on them. Therefore, the IoT system can be effectively simulated and we can find the optimal monitoring cycle to keep the IoT system safe.

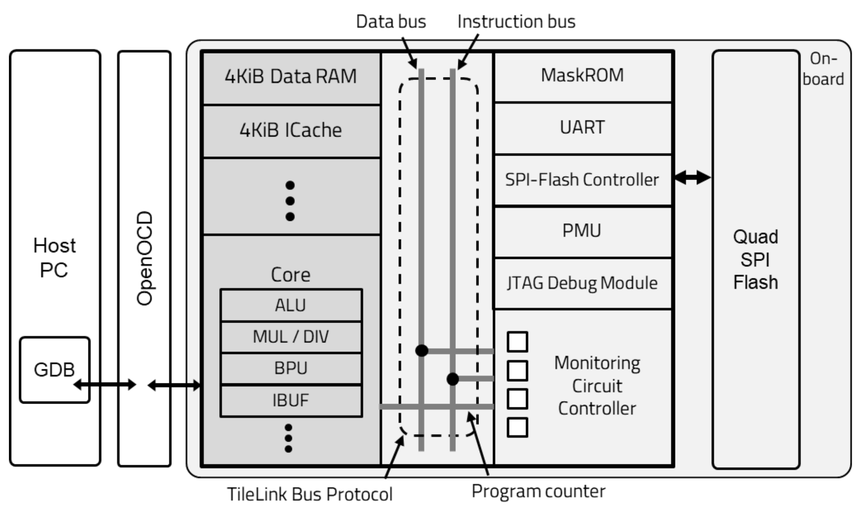
Chisel-based Design

Constructing Hardware in an Scala Embedded Language



Chisel is an open-source hardware construction language developed at UC Berkeley that supports advanced hardware design using highly parameterized generators and layered domain-specific hardware language. Therefore, by designing the hardware of the desired structure through parameterizing the RISC-V architecture based on Chisel, we can efficiently configure optimized hardware for an application

Proposed RISC-V Processor

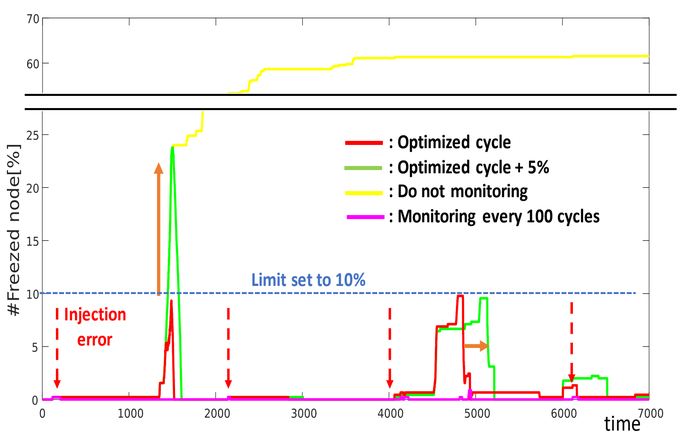


- Magnachip 350nm Process
- ISA: RV32IMAC
- Die size: 5mm x 4mm
- Operating frequency: 25MHz
- Gate count: 110,000 (except memory)

Integrated solution including from SW development environment to HW design

RISC-V is an open-source instruction set architecture (ISA) based on established reduced instruction set computing (RISC) principles. We adopt and reconfigure the freedom e300 platform, which is open-source hardware based on RISC-V and managed by Sifive as a processor to be implemented in ASIC.

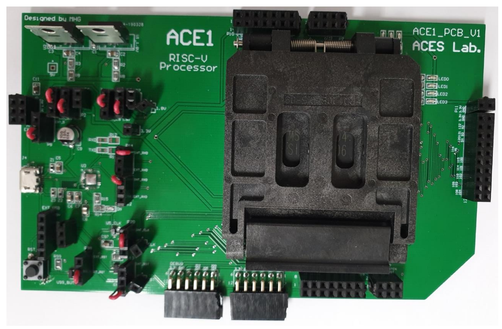
Experiments and Verifications



Left figure shows the results of applying the activation period obtained from the proposed simulation platform to the target IoT system. The errors were injected periodically into selected nodes among the 450 nodes to observe freezing.

When the optimized activation period was applied to each module, we confirmed that the freezing propagation was prevented within the pre-determined tolerance limit of freezing propagation.

Chip name: ACE2 (RISC-V based)
Full-chip simulation: done
Post-layout simulation: done
Supply voltage: 5V (3.3V)
Chip operating result:
Normal operation
(Revision of ACE1)



This chip design is our second general purpose IoT processor. We will develop it toward the application-specific IoT processor in the future.

KNU

IDEC 반도체설계교육센터 IC DESIGN EDUCATION CENTER